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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,266	02/09/2004	Chi-Cheng Ju	3722-0176P	8567

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,266	JU ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 18, 2006 has been entered.

Response to Amendment

2. Applicant's arguments filed August 18, 2006 have been fully considered but they are not persuasive.

3. Applicant argues that to one of ordinary skill in the art, the memory cells within the same row are often collectively referred to as a "page". Applicant has cited his own application for this definition. Vinekar (US005581310A) does not redefine that the odd buffer page and the even buffer page are parts in a single page, according to the definition used in the art of "page" in memory, the odd buffer page and the even buffer page are different pages and cannot be considered as the first memory section and the second memory section in the present invention (pages 7-8).

In reply, the Examiner disagrees. According to *The Authoritative Dictionary of IEEE Standards Terms*, a "page" is a fixed-length segment of data treated as a unit in storage

allocation. Therefore, to one of ordinary skill in the art, the definition of "page" is not necessarily memory cells within the same row. To one of ordinary skill in the art, a "page" is a fixed-length segment of data treated as a unit in storage allocation. The "page" of Vinekar is a fixed-length segment of data treated as a unit in storage allocation (Col. 12, line 46-Col. 13, line 11, Figure 8, 9), and therefore would be considered a "page" to one of ordinary skill in the art.

Applicant argues that the subject invention can outperform the prior art field-organized storage method. Since the top field or bottom field of a macroblock are consecutive addressed in this embodiment, DRAM burst access mode can be used to burst access these top field or bottom field and conceal the next row-activation command overhead cycles during current DRAM burst access (page 11).

In reply, the Examiner points out that Vinekar is addressing a similar problem. Vinekar also describes that in the prior art, conventional data organizations that would employ S-DRAMs have the problem that not every burst mode access will be fully utilized due to conflicting memory access requirements; hence, wasting memory access and bandwidth. Vinekar's invention solves the problem of the access inefficiencies due to conflicting access requirements of a macroblock-based frame reconstruction circuit, and the memory is amenable to implementation with S-DRAM circuits (Col. 4, lines 11-29). The odd and even data are organized in such a way so that no loss in memory throughput results therefrom (Col. 13, lines 1-12, 24-42).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-4 and 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGuinness (US006104416A) in view of Vinekar (US005581310A).

7. With regard to Claim 1, McGuinness describes a method of storing an array of digital data into a memory (Col. 3, lines 14-16) having a plurality of memory pages (Col. 8, lines 51-58), the method comprising the steps of dividing the array of digital data into a plurality of block units (Col. 3, lines 16-18) each of the block units having a plurality of odd rows and a plurality of even rows (Col. 11, line 51-Col. 12, line 13), each of the odd rows and the even rows having at least one byte (*one byte of storage is required for each pixel*, Col. 4, lines 47-48; *putting 16*

pixels into each row, Col. 11, lines 52-54); storing subsequent odd rows of at least one of the block units into consecutive storage locations in the first memory section (532) (Col. 11, lines 57-63), and storing subsequent even rows of at least one of the block units into consecutive storage locations in the second memory section (534) (Col. 11, line 65-Col. 12, line 13).

However, McGuinness does not specifically teach that at least one memory page has the first memory section and the second memory section. However, Vinekar describes that each bank contains an odd buffer page section and an even buffer page section (Col. 12, line 46-Col. 13, line 11, Figure 8, 9). These sections are labeled "odd buffer **page 0**" and "even buffer **page 0**", which means that these odd and even sections are on the same page 0, so Bank 0 (800) is considered to contain one page, page 0. Therefore, Vinekar discloses that at least one memory page (page 0, 800) has a first memory section (odd buffer page 0) and a second memory section (even buffer page 0).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of McGuinness so that at least one memory page has the first memory section and the second memory section as suggested by Vinekar because Vinekar suggests the advantage of fully utilizing every burst mode access, therefore increasing bandwidth and thus being capable of operating at very high data transfer rates expected in high performance video applications (Col. 4, lines 11-29).

8. With regard to Claim 2, McGuinness describes that the array of digital data comprises a picture in a video bit stream (Col. 4, line 64-Col. 5, line 9).

9. With regard to Claim 3, McGuinness describes that the first memory section (532) has a first number of first areas (words) and the second memory section (534) has a second number of second areas, each of the first areas and the second areas has consecutive storage locations, each of the first number and the second number is equal to or larger than one (Col. 11, line 55-Col. 12, line 4).

10. With regard to Claim 4, McGuinness discloses that the first number is equal to the second number (Col. 11, line 55-Col. 12, line 4), as shown in Figure 8.

11. With regard to Claim 6, McGuinness discloses that both the first number and the second number can inherently be modified to equal any number (Col. 11, line 55-Col. 12, line 4), and therefore the both the first number and the second number can have a value of one.

12. With regard to Claim 7, McGuinness discloses that both the first number and the second number can inherently be modified to equal any number (Col. 11, line 55-Col. 12, line 4), and therefore the both the first number and the second number can have a value of two.

13. With regard to Claim 8, McGuinness describes that each of the block units has m rows, wherein m is an integer equal to or larger than four (Col. 10, lines 43-53).

14. With regard to Claim 9, McGuinness describes that m is equal to thirty-two (Col. 10, lines 43-53).

15. With regard to Claim 10, Claim 10 is similar in scope to Claims 1 and 2, and therefore is rejected under the same rationale. With regard to Claims 11 and 12, these claims are similar in scope to Claims 3 and 8 respectively, and therefore are rejected under the same rationale.

16. With regard to Claim 13, Claim 13 is similar in scope to Claim 1, except for the addition of retrieving a prediction block of picture from the memory, retrieving the digital data representing the prediction block stored in the first memory section, and retrieving the digital data representing the prediction block stored in the second memory section. McGuinness describes retrieving a prediction block of picture from the memory, retrieving the digital data representing the prediction block stored in the first memory section (532, Figure 8), and retrieving the digital data representing the prediction block stored in the second memory section (534) (Col. 7, lines 64-67; Col. 11, line 51-Col. 12, line 32). Therefore, Claim 13 is rejected under the same rationale as Claim 1.

17. With regard to Claims 14 and 15, these claims are similar in scope to Claims 3 and 8 respectively, and therefore are rejected under the same rationale.

Prior Art of Record

Breitfelder, Kim; Messina, Don. *The Authoritative Dictionary of IEEE Standards Terms*. 2000. IEEE Press. Seventh Edition. p. 789.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER